

FIG. 1

| | |
|----------------------|----------------------|
| 110 <i>ADDR 0</i> | 120 <i>DATA 0</i> |
| <i>ADDR 1</i> | <i>DATA 1</i> |
| • • • | |
| <i>ADDR N</i> | <i>DATA N</i> |

FIG. 2

| | | |
|----------------------|----------------------|--------------------------|
| 110 <i>ADDR 0</i> | 120 <i>DATA 0</i> | 130 <i>BUS TYPE 0</i> |
| <i>ADDR 1</i> | <i>DATA 1</i> | <i>BUS TYPE 1</i> |
| • • • | | |
| <i>ADDR N</i> | <i>DATA N</i> | <i>BUS TYPE N</i> |

FIG. 3

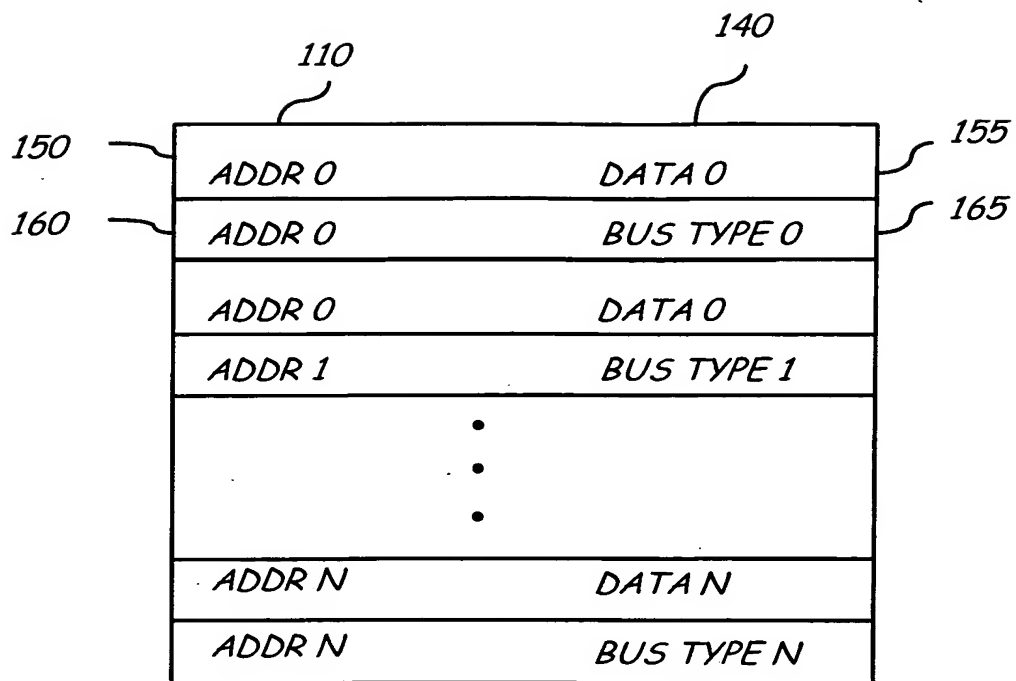


FIG. 4

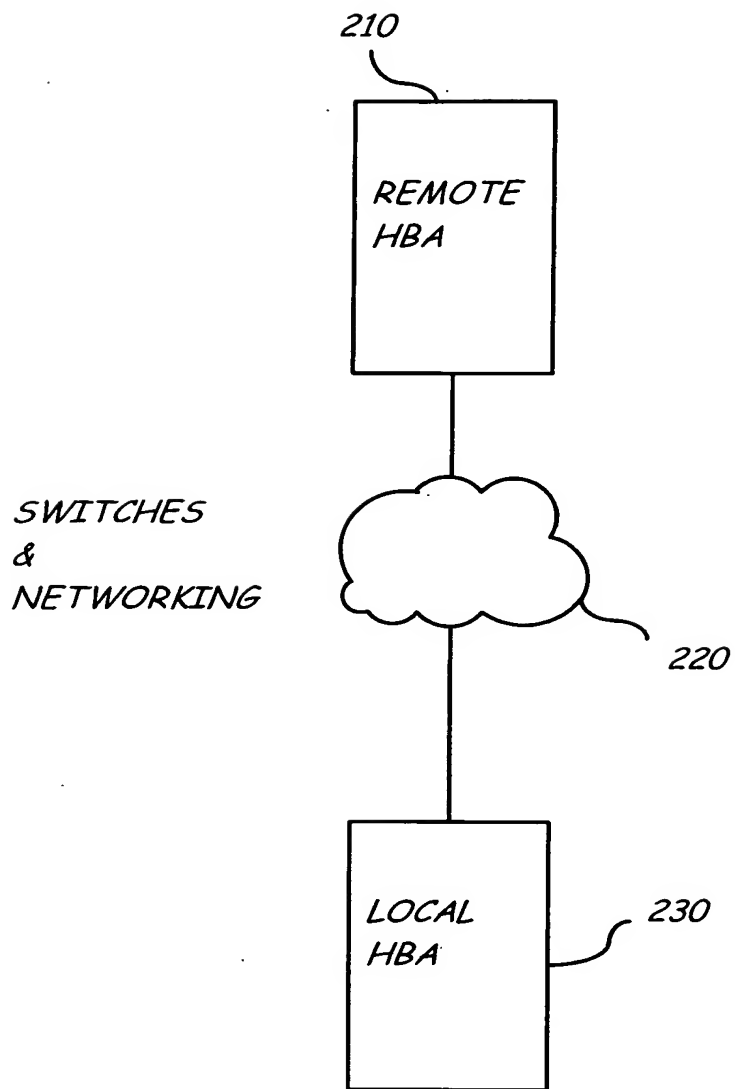


FIG. 5

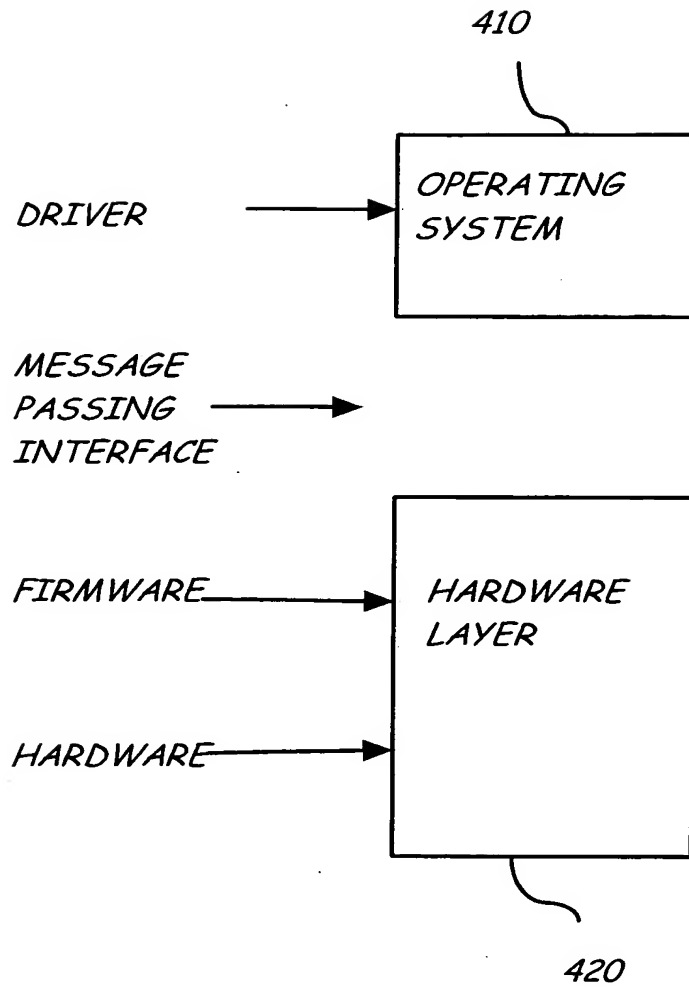


FIG. 6

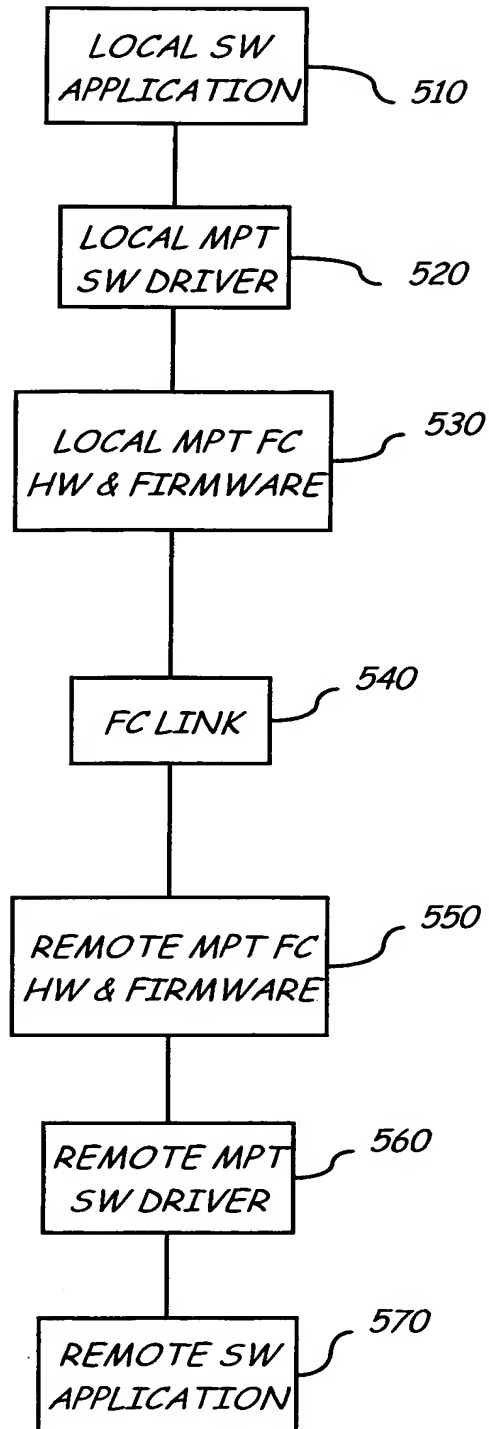


FIG. 7

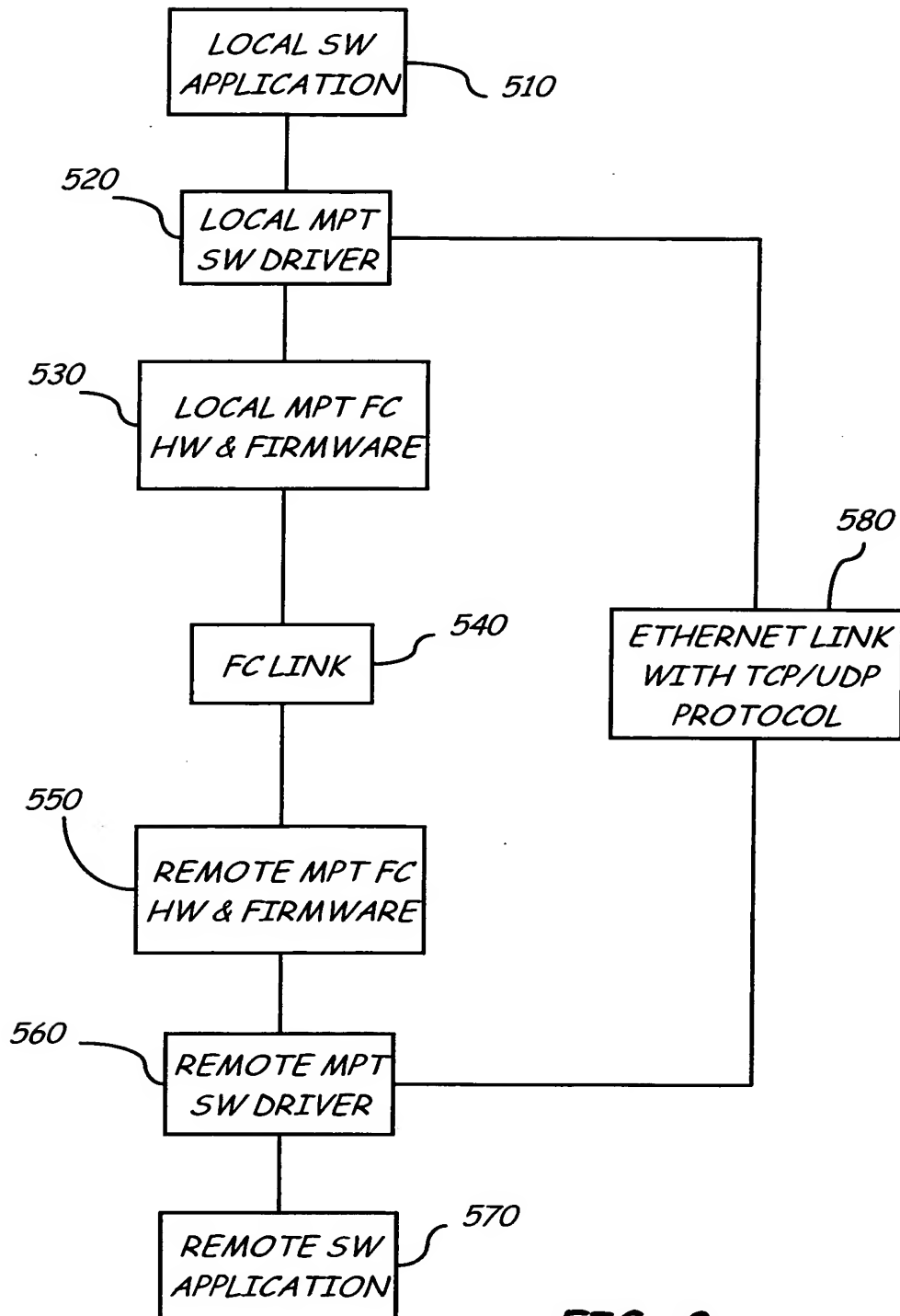


FIG. 8